

Vassilis Paliouras is an Associate Professor at the Electrical and Computer Engineering Department, University of Patras, Greece. His research interests are in the areas of VLSI Digital Signal Processing hardware architectures with emphasis on baseband processing, error correction coding and iterative decoders, variation-tolerant hardware architectures, low-power hardware architectures and computer arithmetic. He has published more than 130 articles, in international journals, conferences, book chapters and has edited four books. He is a co-author of a textbook and inventor to four US patents. He is/has been advisor to five PhD theses and 28 master and 30 diploma theses. He has received a best-paper award for an IEEE Transactions on Circuits and Systems publication. He has been the general chair of *International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS 2004)* and currently serves as PATMOS steering committee manager. He has been technical program chair for the *PATMOS 2005*, *IEEE Workshop on Signal Processing Systems Implementation (SIPS) 2005*, *IEEE International Conference on Electronics Circuits and Systems (ICECS) 2010* as well as European liaison for IEEE ISCAS 2012, Korea. Also he is an associate editor for IET Circuits, Devices & Systems, and has served in the boards of IEEE Signal Processing Letters, IEEE Transactions on Circuits and Systems – Part I, and as guest editor for the Journal of Low-power electronics. He is a member of the technical program committee in a large number of conferences in the areas of circuits and systems, digital signal processing and telecommunications. He is/has been a principal investigator in several research projects, focusing on baseband hardware (FPGA and ASIC), for wireless communications applications in the 60 GHz band, wifi hardware, and specialized hardware for error correction based on LDPC, Reed-Solomon, and convolutional codes. R&D efforts involve development of prototypes for communications baseband digital hardware. Other projects focus on the design of fault-tolerant systems, under soft errors.

Detailed info: <http://www.ics.ece.upatras.gr/people/vassilis-paliouras/>